REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-7, 9-11, 13, 15-22 and 24-36 were pending and rejected. Claims 11, 13, and 15-19 are allowed. Claims 5-7, 10-11, 20, 25-27, 30-31, and 33-35 have been amended. Claims 37-44 have been added. No new matter has been added.

Allowable Claims

Applicants would like to gratefully acknowledge the Examiner's indication that claims 11, 13, 15-19 would be allowable if the objection to claim 11 were overcome. Claim 11 has been amended as suggested to overcome the objection. The Applicants submit that claim 11 and the respective dependent claims are allowable. Therefore, the Applicants respectfully request that the Examiner withdraw the objection to claims 11, 13, 15-19.

Amendment to Specification

The title of the specification was rejection in the Office Action. The title has been replaced with "A multithreaded processor capable of implicit multithreaded execution of a single-threaded program". Applicants respectfully request the objection to be withdrawn.

Claim Objections

Claims 5-7, 10-11, 30-31, and 33-35 have been objected to because of informalities in the Office Action. The claims have been amended as suggested. Applicants respectfully request the objections towards the claim to be withdrawn.

Claim 20 has been objected to because of informalities in the Office Action. In this response, line 8 of the claim has been amended as suggested. Line 4 and Line 5 of claim 20 have been amended to recite "executing a single thread by a first processor; executing said

single thread from by a second processor as directed by the first ..." Applicants respectfully submit that the claim is clear and concise in regards to the subject matter which Applicants regard as the invention. Applicants respectfully request the objection towards the claim to be withdrawn.

Claim Rejection – 35 U.S.C. §101

Claims 20-22 and 24-28 are rejected under 35 U.S.C. §101. Applicants submit that the machine-readable media in the claims do not include propagation signals. Applicants submit that the claim 20 and its dependent claims 21-22, 24-28 are directed to the statutory matters as required by 35 U.S.C. §101. The Applicants respectfully request the rejections towards the claims to be withdrawn.

Claim Rejection – 35 U.S.C. §103

The following discussion sets forth in detail Applicants' analysis with respect to the patentability of claims 1-7, 9-10 and 29-36.

A. It is asserted in the Office Action that claims 1-7, 9-10 and 29-36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nair et al., U. S. Patent 7,017,073 (hereinafter Nair '073) in view of Hennessy and Patterson ("Computer Architecture A Quantitative Approach", Morgan Kaufmann, 1996) (hereinafter "Hennessy"), and Sundaramoorthy et al. ("Slipstream Processors: Improving both Performance and Fault Tolerance", ASPLOS, pp. 257-268, Nov. 2000) (hereinafter "Sundaramoorthy"). Applicants respectfully traverse the aforementioned rejections for the following reasons.

Applicants would like to point out that Nair '073 claims priority to a provisional application 60/272,138 filed on Feb 28, 2001 (hereinafter Nair '138). Nair '073 and Nair '138 do not have the same specification. The filing date of Nair '073, Feb 27, 2002, is later than the

filing date of Applicants' application (i.e., June 28, 2001). Applicants submit that it is improper to use Nair '073 as a reference in the Office Action.

Claim 1 recites:

> 1. An apparatus comprising:
> a first processor and a second processor each having a scoreboard and a decoder;
> **a plurality of memory devices coupled to the first processor and the second processor;**
> **a first buffer coupled to the first processor and the second processor, the first buffer being a register buffer and is operable to transfer register values from the second processor to the first processor**;
> a second buffer coupled to the first processor and the second processor, the second buffer being a trace buffer; and
> a plurality of memory instruction buffers coupled to the first processor and the second processor;
> wherein the first processor and the second processor perform single threaded applications using multithreading resources, and the first processor executes a single threaded application ahead of the second processor executing said single threaded application to avoid misprediction, said single threaded application is not converted to an explicit multiple-thread application, said single threaded application contains the same number of instructions when executed on said first processor and said second processor, and the single threaded application executed on the second processor avoids branch mispredictions from information received from said first processor. (emphasis added)

Applicants submit that Nair '138, Sundaramoorthy, and Hennessy fail to disclose at least the two limitations of claim 1.

Nair '138 describes performing fault checking by comparing results of a foreground thread (i.e., A) in a processor and results of a check thread (i.e., A') in another processor (Nair '138, page 2, paragraph 2). Nair '138 states that check thread (A') naturally tend to run more slowly (Nair '138, page 2, paragraph 3). Nair '138 also suggests that foreground thread A will be forced to slow down because of the speed mismatch between A and A'. Nair is silent about disclosing "a plurality of memory devices coupled to the first processor and the second processor". The Office Action also admits that Nair fails to disclose "a first buffer coupled to

the first processor and the second processor, the first buffer being a register buffer and is operable to transfer register values from the second processor to the first processor."

Sundaramoorthy discloses a multiprocessor system that executes two (i.e., multiple streams/threads) pseudo-redundant programs on separate processors on the same chip. Claim 1 requires "a first buffer coupled to the first processor and the second processor, the first buffer being a register buffer and is operable to transfer register values from the second processor to the first processor", where the first processor executes a single threaded application ahead of the second processor as recited in claim 1. The Office Action alleges that "a first buffer" is disclosed by the delay buffer in Sundaramoorthyin (Fig. 1 and col. 10, lines 17-21). Applicants respectfully disagree. Sundaramoorthy states that "the delay buffer is a simple FIFO queue that allows the A-stream to communicate control flow and data flow outcomes to the R-stream." Sundaramoorthy defines that "the leading program is called the advanced stream, or A-stream, and the trailing program is called the redundant stream, or R-stream." (col. 2, lines 4-6). Sundaramoorthy discloses a delay buffer that allows the advance stream to communicate control flow and data flow from A-stream to R-stream (not the other way around). In short, a delay buffer is not the first buffer as claimed in claim 1. Sundaramoorthy fails to disclose the limitation as required. Sundaramoorthy also fails to mention "a plurality of memory devices coupled to the first processor and the second processor".

Hennessy discloses using score boarding to aid in allowing instructions to execute out of order. Hennessy is also silent with respect to disclosing "a plurality of memory devices coupled to the first processor and the second processor" and "a first buffer coupled to the first processor and the second processor, the first buffer being a register buffer and is operable to transfer register values from the second processor to the first processor."

In short, Nair '138 in view of Sundaramoorthy and Hennessy fail to disclose all limitations as required in claim 1.

Moreover, it is asserted in the Office Action it would be obvious to combine Nair '138 with Sundaramoorthy in order to speed up execution of a trailing thread (Office Action, page 7, lines 9-10). As explained above, however, check thread (A'), which is the trailing thread,

naturally tend to run more slowly (Nair '138, page 2, paragraph 3). As stated in MPEP 2143.01 (VI), the proposed modification can not change the principle of operation of a reference. "*If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious.*" Applicants submit that the combination proposed in the Office Action contradicts to the principle of Nair '138. Therefore, the combination fails to establish a prima facie case with respect to claim 1.

At least for the foregoing reasons, Applicants submit that claim 1 is not obvious over Nair '138, Sundaramoorthy, and Hennessy. Applicants respectfully request the withdrawal of the rejection for claim 1. Claims 2-7, and 9-10 depend from claim 1 are therefore also allowable. Applicants respectfully request the withdrawal of the rejection for the claims.

Claim 29, as amended, recites:

> 29. (Currently Amended) A system comprising:
> a first processor and a second processor each having a scoreboard and a decoder;
> a bus coupled to the first processor and the second processor;
> a main memory coupled to the bus;
> a plurality of local memory devices coupled to the first processor and the second processor;
> a first buffer coupled to the first processor and the second processor, the first buffer being a register buffer and is operable to transfer register values from the second processor to the first processor;
> **a second buffer coupled to the first processor and the second processor, the second buffer being a trace buffer; and**
> a plurality of memory instruction buffers coupled to the first processor and the second processor,
> wherein the first processor and the second processor perform single threaded applications using multithreading resources, the second processor executes a single threaded application ahead of the first processor executing said single threaded application to avoid misprediction, **wherein the first processor avoid executing a portion of instructions by committing results of a portion of the plurality of instructions into a register file from the second buffer**. (Emphasis added)

In the section of allowable subject matter, the Office Action indicates that the references fail to disclose at least "the first processor avoiding executing a portion of instructions by committing the results of the portion of instructions into a register file from a

first buffer". Claim 29 requires at least the same limitation. For at least the same reason, Applicants respectfully submit that claim 29 is not obvious over the cited references. Claims 30-31 and 33-36 depend from amended claims 29, are also not obvious over the references for the same reason. Accordingly, Applicants respectfully request the withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 29-31 and 33-36.

The following discussion sets forth in detail Applicants' analysis with respect to the patentability of claims 20-22, and 24-28.

B. It is asserted in the Office Action that claims 20-22, and 24-28 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nair '073 in view of Hennessy, Sundaramoorthy, Akkary (WO 99/31594), and Tanenbaum "Structured Computer Organization," Prentice-Hall, 1984, pp. 10-12 ("Tanenbaum").

Claim 20, as amended, contains the limitations of

> 20. An apparatus comprising a machine-readable storage medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising:
> executing a single thread by a first processor;
> executing said single thread by a second processor as directed by the first processor, the second processor executing instructions ahead of the first processor to avoid misprediction;
> tracking at least one register that is one of loaded from a register file buffer and written by said second processor, said tracking executed by said second processor;
> **transmitting results from the second processor to the first processor, the first processor avoiding executing a portion of instructions by committing the results of the portion of instructions into a register file from a first buffer, the first buffer being a trace buffer; and**
> clearing a store validity bit and setting a mispredicted bit in a load entry in the first buffer if a replayed store instruction has a matching store identification (ID) portion in a second buffer, the second buffer being a load buffer,
> wherein the first processor and the second processor execute single threaded applications using multithreading resources, said single thread is not converted to an explicit multiple-thread application, said single thread contains the same number of instructions when executed on said first processor and said second processor, and said single thread executed on the second processor avoids branch

mispredictions using information received from said first processor. (Emphasis added)

In the section of allowable subject matter, the Office Action indicates that the references fail to disclose at least "the first processor avoiding executing a portion of instructions by committing the results of the portion of instructions into a register file from a first buffer". Claim 20 requires at least the same limitation. For at least the same reason, Applicants respectfully submit that claim 20 is not obvious over the cited references. Claims 21-22 and 24-28 depend from amended claims 20 are also not obvious over the references for the same reason. Accordingly, Applicants respectfully request the withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 20-22, 24-28.

New Claims

Applicants present new claims (claims 37-44). Claim 37 is an independent claim. Claims 38-44 depend from claim 37.

Claim 37 requires "wherein the first processor and the second processor execute single threaded applications using multithreading resources, and the second processor is operable to execute a single threaded application ahead of the first processor executing said single threaded application to avoid misprediction, wherein the first processor avoids executing a portion of instructions by committing results of the portion of the instructions into a register file from the second buffer". In the section of allowable subject matter, the Office Action indicates that the references fail to disclose at least "the first processor avoiding executing a portion of instructions by committing the results of the portion of instructions into a register file from a first buffer". For at least the same reason, Applicants respectfully submit that claim 37 is not obvious over the cited references. Claims 38-44 depend from claim 37 are therefore also allowable. Applicants respectfully request the allowance for claim 37-44.

CONCLUSION

Applicants respectfully request the amendments of claims to be admitted. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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